

Document Title**512Kx8 bit Low Power CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	December 7, 1996	Advance
0.1	Revise - Changed Operating current by reticle revision Icc at write : 35mA → 45mA Icc1 at read/write : 15/35mA → 10/45mA	March 6, 1997	Preliminary
1.0	Finalize - Changed Operating current Icc1 at write : 45mA → 40mA Icc2; 90mA → 80mA - Change test load at 55ns : 100pF → 50pF	October 9, 1997	Final
2.0	Revise - Change datasheet format	February 17, 1998	Final
3.0	Revise - Industrial product speed bin change:70/100ns → 55/70ns	September 8, 1998	Final

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512Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 512Kx8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-DIP-600, 32-SOP-525
32-TSOP2-400F/R

GENERAL DESCRIPTION

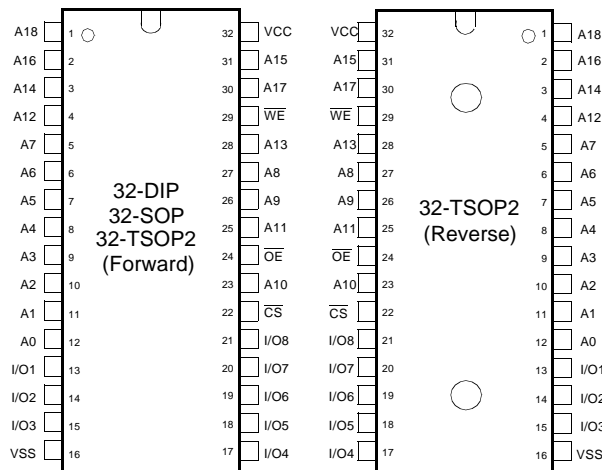
The K6T4008C1B families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
K6T4008C1B-L K6T4008C1B-B	Commercial (0~70°C)	4.5~5.5V	55 ¹⁾ /70ns	100µA 20µA	80mA	32-DIP-600, 32-SOP-525 32-TSOP2-400F/R
K6T4008C1B-P K6T4008C1B-F				100µA 50µA		

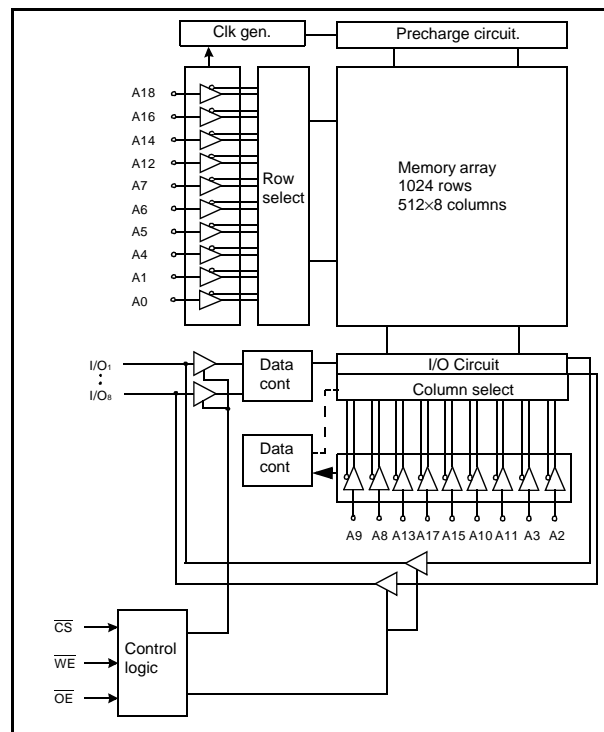
1. The parameter is measured with 50pF test load.

PIN DESCRIPTION



Pin Name	Function
\overline{WE}	Write Enable Input
\overline{CS}	Chip Select Input
\overline{OE}	Output Enable Input
A0~A18	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
K6T4008C1B-DL55	32-DIP, 55ns, L-pwr	K6T4008C1B-GP55	32-SOP, 55ns, L-pwr
K6T4008C1B-DB55	32-DIP, 55ns, LL-pwr	K6T4008C1B-GF55	32-SOP, 55ns, LL-pwr
K6T4008C1B-DL70	32-DIP, 70ns, L-pwr	K6T4008C1B-GP70	32-SOP, 70ns, L-pwr
K6T4008C1B-DB70	32-DIP, 70ns, LL-pwr	K6T4008C1B-GF70	32-SOP, 70ns, LL-pwr
K6T4008C1B-GL55	32-SOP, 55ns, L-pwr	K6T4008C1B-VF55	32-TSOP2-F, 55ns, LL-pwr
K6T4008C1B-GB55	32-SOP, 55ns, LL-pwr	K6T4008C1B-VF70	32-TSOP2-F, 70ns, LL-pwr
K6T4008C1B-GL70	32-SOP, 70ns, L-pwr	K6T4008C1B-MF55	32-TSOP2-R, 55ns, LL-pwr
K6T4008C1B-GB70	32-SOP, 70ns, LL-pwr	K6T4008C1B-MF70	32-TSOP2-R, 70ns, LL-pwr
K6T4008C1B-VB55	32-TSOP2-F, 55ns, LL-pwr		
K6T4008C1B-VB70	32-TSOP2-F, 70ns, LL-pwr		
K6T4008C1B-MB55	32-TSOP2-R, 55ns, LL-pwr		
K6T4008C1B-MB70	32-TSOP2-R, 70ns, LL-pwr		

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	I/O Pin	Mode	Power
H	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	High-Z	Output disbaled	Active
L	L	H	Dout	Read	Active
L	X ¹⁾	L	Din	Write	Active

1. X means don't care.(Must be in low or high state.)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} ,V _{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	K6T4008C1B-L/-B
		-40 to 85	°C	K6T4008C1B-P/-F
Soldering temperature and time	T _{SOLDER}	260°C, 10sec(Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.5 ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

Note:

- Commercial Product: T_A=0 to 70°C, otherwise specified
Industrial Product: T_A=-40 to 85°C, otherwise specified
- Overshoot: V_{CC}+3.0V in case of pulse width ≤ 30ns
- Undershoot: -3.0V in case of pulse width ≤ 30ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

- Capacitance is sampled, not 100% tested

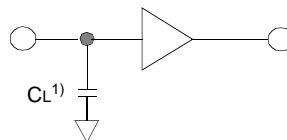
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IL} or V _{IH} , Read	-	7.5	15	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS} \leq 0.2V$, V _{IN} ≥ 0.2V or V _{IN} ≥ V _{CC} -0.2V	Read	-	4	10	mA
			Write	-	27	40	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}=V_{IL}$, V _{IN} =V _{IH} or V _{IL}	-	65	80	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}=V_{IH}$, Other inputs = V _{IL} or V _{IH}	-	-	3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, Other inputs=0-V _{CC}	K6T4008C1B-L	-	2	100	μA
			K6T4008C1B-B	-	1	20	μA
			K6T4008C1B-P	-	2	100	μA
			K6T4008C1B-F	-	1	50	μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level: 0.8 to 2.4V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load (See right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L=50\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC}=4.5\sim 5.5\text{V}$, Commercial product: $T_A=0$ to 70°C , Industrial product: $T_A=-40$ to 85°C)

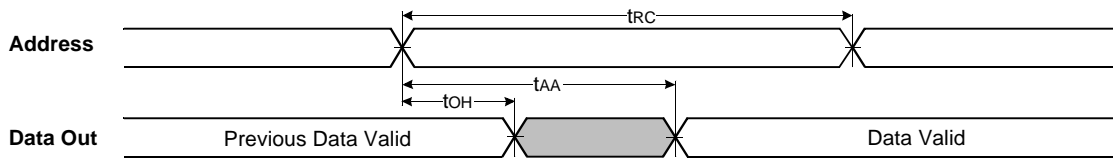
Parameter List		Symbol	Speed Bins				Units
			55*ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	20	0	25	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	25	ns
	Output hold from address change	t _{OH}	10	-	10	-	ns
Write	Write cycle time	t _{WC}	55	-	70	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	ns
	Write pulse width	t _{WP}	40	-	50	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	25	ns
	Data to write time overlap	t _{DW}	25	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

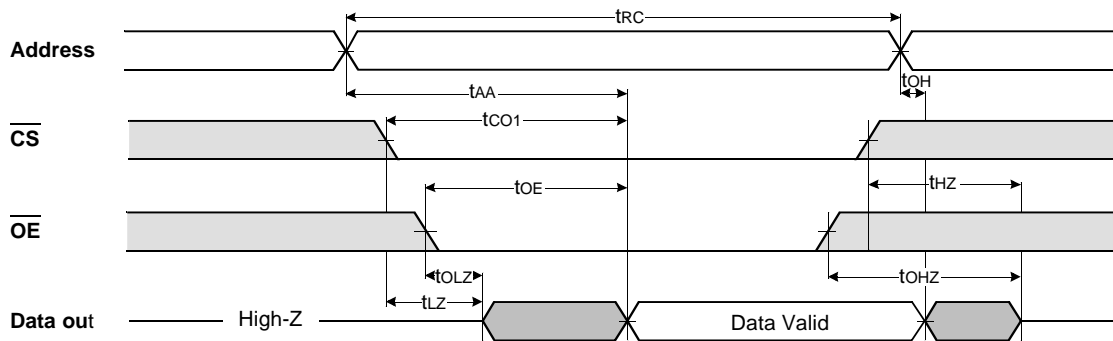
Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V _{CC} for data retention	V _D R	$\overline{CS} \geq V_{CC}-0.2\text{V}$	2.0	-	5.5	V	
Data retention current	I _D R	$V_{CC}=3.0\text{V}, \overline{CS} \geq V_{CC}-0.2\text{V}$	K6T4008C1B-L	-	-	50	μA
			K6T4008C1B-B	-	-	15	
			K6T4008C1B-P	-	-	50	
			K6T4008C1B-F	-	-	20	
Data retention set-up time	t _{SD} R	See data retention waveform	0	-	-	ms	
Recovery time	t _R D		5	-	-		

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



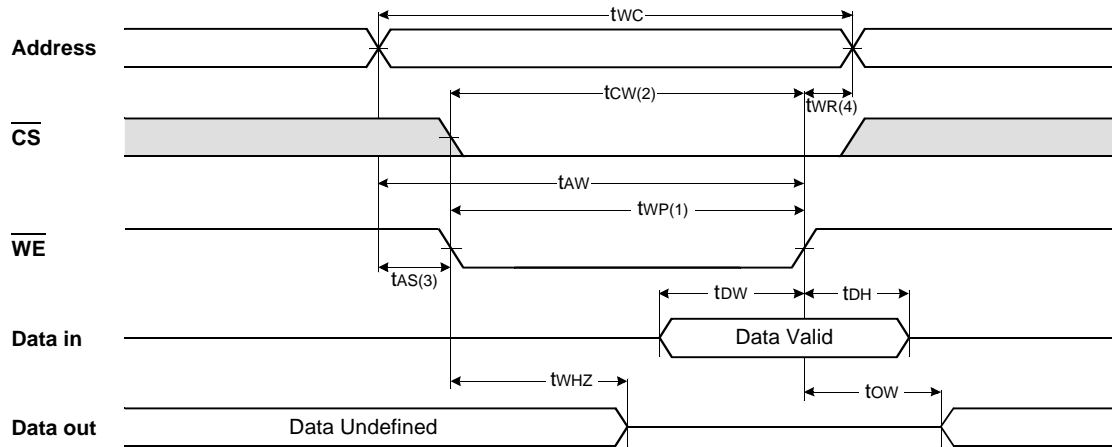
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



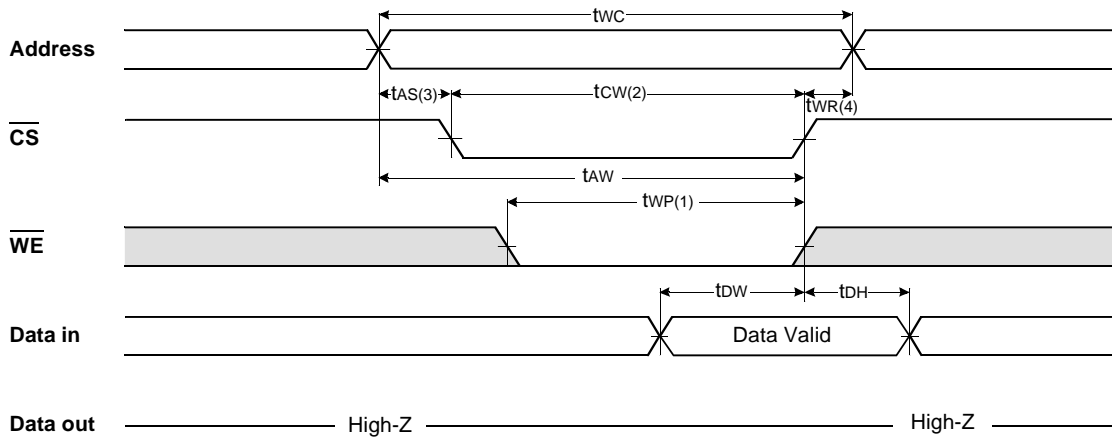
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{CS} Controlled)

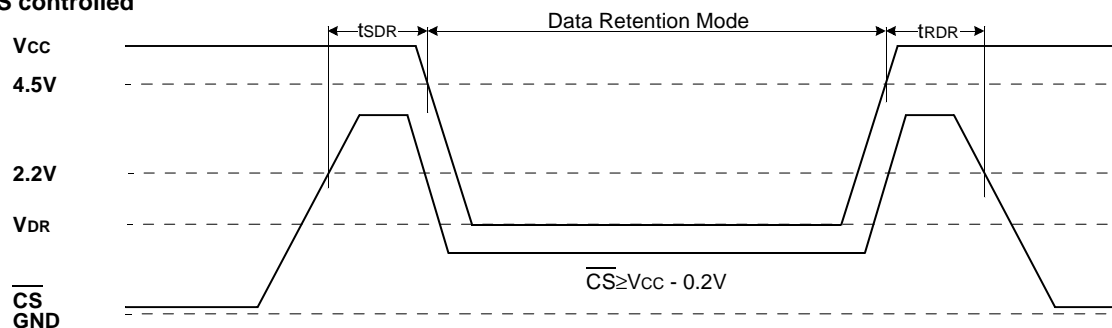


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . A write begins at the latest transition among \overline{CS} going Low and \overline{WE} going low : A write end at the earliest transition among \overline{CS} going high and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as \overline{CS} or \overline{WE} going high.

DATA RETENTION WAVE FORM

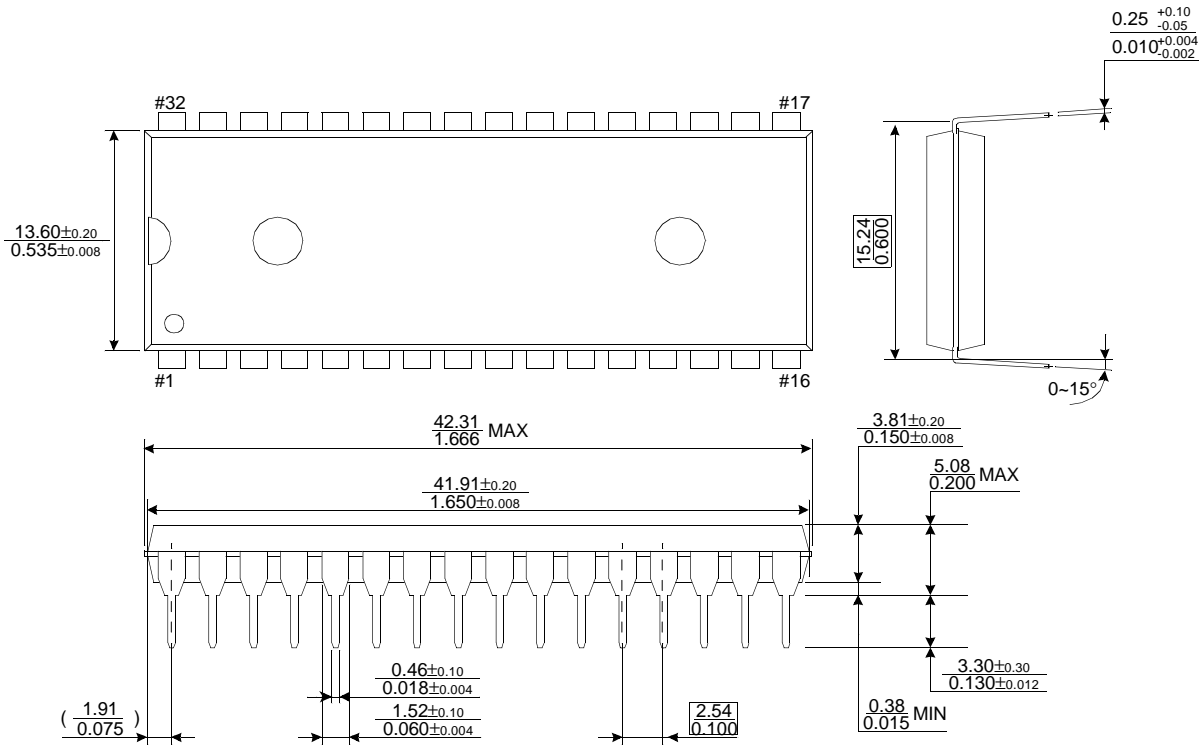
\overline{CS} controlled



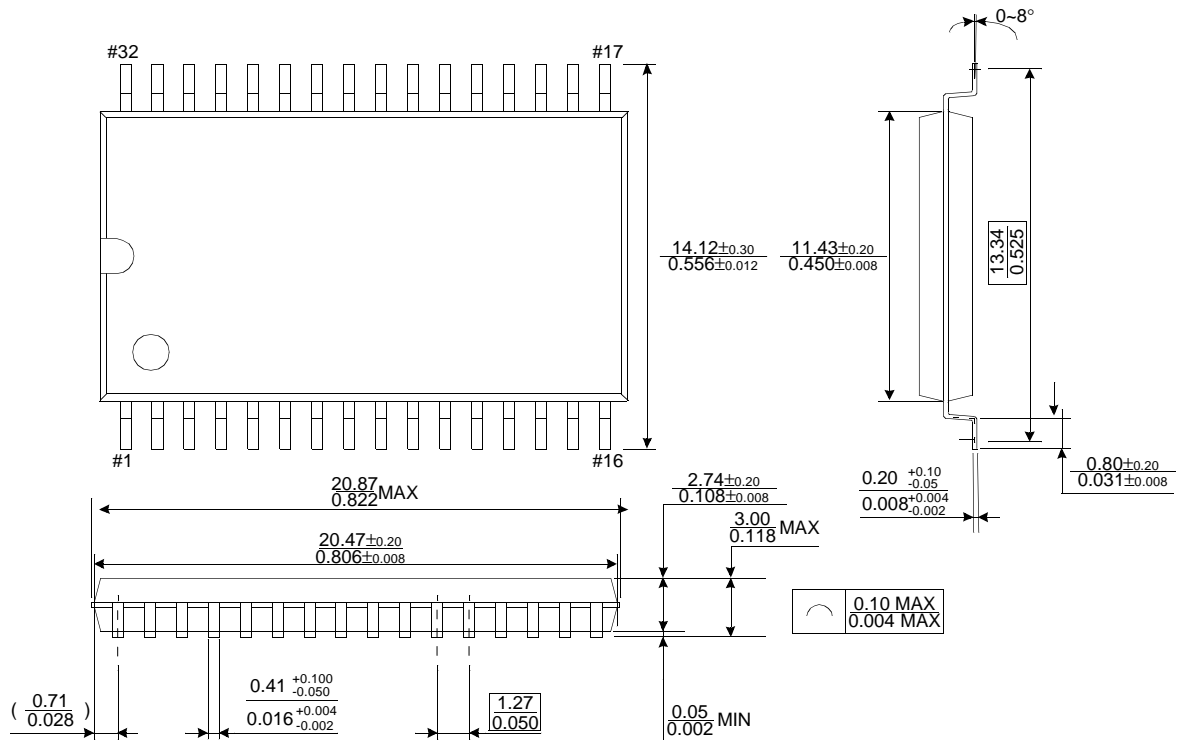
PACKAGE DIMENSIONS

Units: millimeter(Inch)

32 PIN DUAL INLINE PACKAGE (600mil)



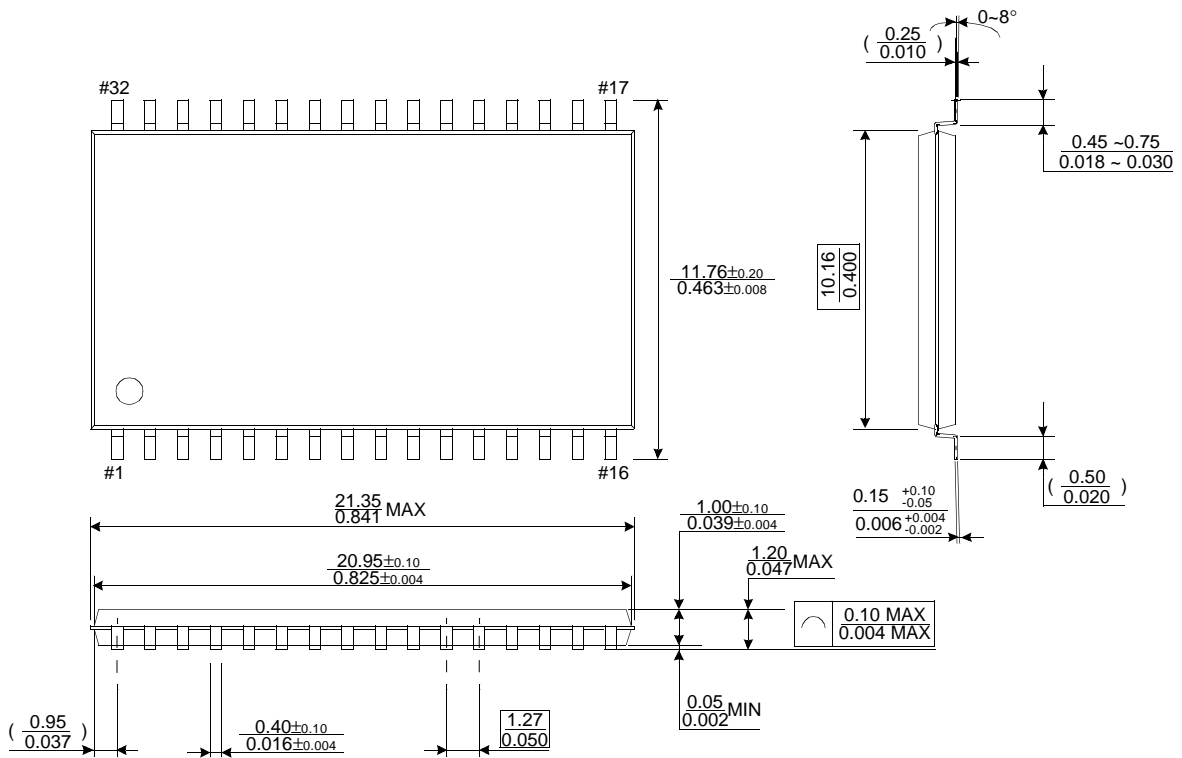
32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



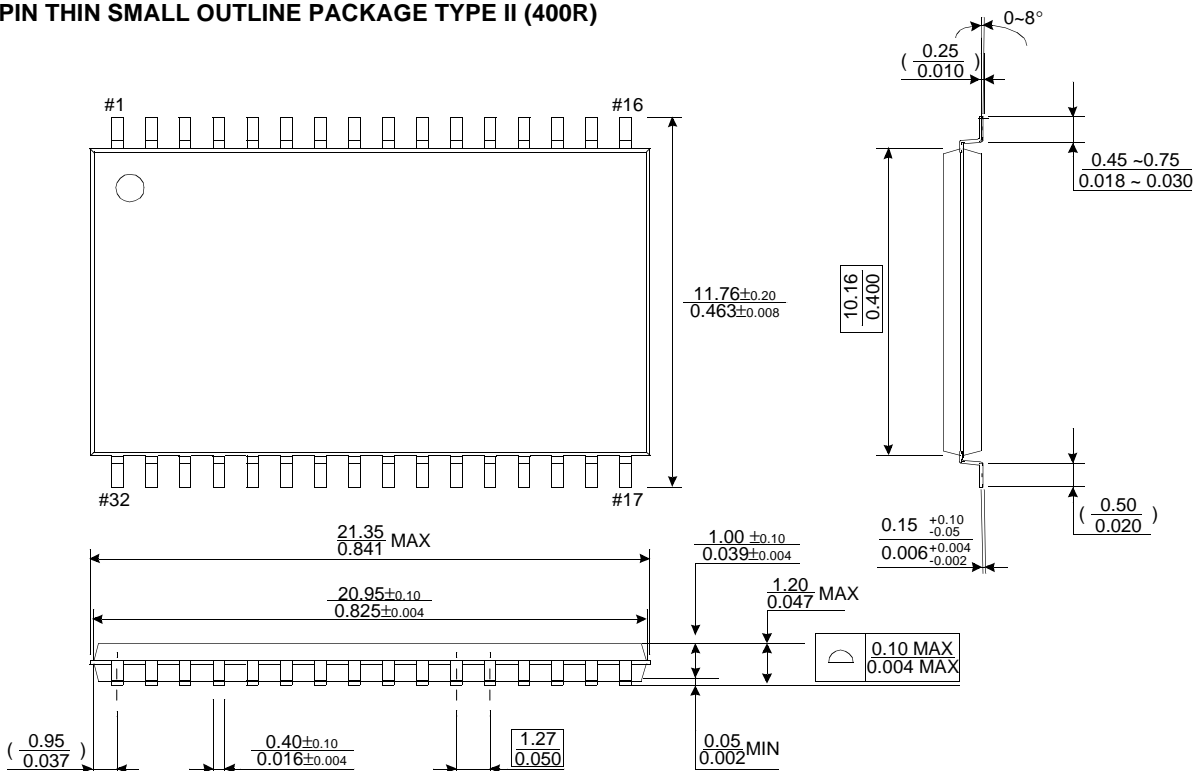
PACKAGE DIMENSIONS

Units: millimeter(Inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)



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